REMARKS/ARGUMENTS

This Amendment is responsive to the Office Action mailed on January 29, 2003. A petition for a 1-month extension of time is attached so that the due date is extended to and including May 29, 2003.

A Declaration Pursuant to 37 CFR 1.131 by Ruben Madrid (with Exhibits A-C) is attached. Entry of the Declaration is respectfully requested.

Prior to this Amendment, claims 1-23, 25, and 28 were previously canceled, and claims 24, 26, 27, and 29-37 were pending. In this Amendment, claims 33 and 35 are canceled, and no claims are amended so that claims 24, 26, 27, 29-32, 34, and 36-37 are pending and subject to examination.

In the Office Action, claims 24, 26, 27, 29-33, and 35-37 are rejected as being anticipated by Tan et al. (US 2002/0074147A1). Claim 34 is rejected as obvious over Tan et al. and Shrier et al. (US 2002/0050912 A1). These rejections are traversed.

Tan et al., the only reference cited in the anticipation rejection and the primary reference cited in the obviousness rejection, was filed on December 15, 2000. When any claim of an application is rejected, the inventor of the subject matter of the rejected claim may submit an appropriate oath or declaration to establish invention of the subject matter of the rejected claim prior to the effective date of the reference or activity on which the rejection is based. 37 CFR 1.131(a). "The showing of facts shall be such, in character and weight, as to establish reduction to practice prior to the effective date of the reference..." 37 CFR 1.131(b). As evidenced by the attached Declaration Pursuant to 37 CFR 1.131 by Ruben Madrid, the inventions of the pending claims were reduced to practice in a WTO country prior to December 15, 2000, the effective date of the Tan et al. application. (Pursuant to MPEP § 715.07, the dates on Exhibits A-C have been removed, and the Declaration provides a statement that the acts referred to occurred before December 15, 2000.) Mr. Madrid states the following at paragraph 6 of the attached Declaration:

> As shown by Exhibits A-C, I believe that at least pending claims 24, 26, 27, 29, 30-32, 34, and 36-37 were reduced to practice prior to December 15, 2000, the filing date of U.S. Patent Publication No. 2002/0074147A1 (Tan et al.).

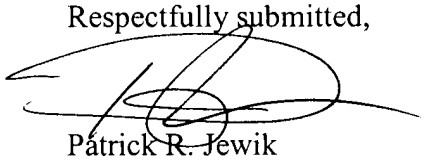
Facts and evidence supporting this conclusion are provided in the Declaration. In view of the Declaration, the Tan et al. patent application is no longer prior art and withdrawal of the prior art rejections is requested.

CONCLUSION

In view of the foregoing, Applicant believes all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



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Application of Copper Bump Leadframe to MosFet BGA Technology

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Abstract

The design concept of "Copper Bump Leadframe" is a result of stamping a flat, thermally and electrically conductive substrate copper material to form the leadframe with built-in copper bump.

The existing technology makes use of solder ball bump as the electrical interconnect in Ball Grid Array (BGA) packages. The process is widely known in the semiconductor industry as balls attach method. However, various manufacturing issues take place in the integrity and quality of ball attachment. These quality issues of ball attach creates reliability failures during board application.

The "Copper Bump Leadframe" was conceptualized for robust bumps interconnect technology for MosFet BGA. The copper bump concept may also replace the traditional solder ball attach method and simplified the process of BGA packages.

The qualification results show an almost perfect coplanarity of copper bump. The electrical (RdSon) results for copper bump is comparable to solder ball bump. It is therefore concluded that the "Copper Bump Leadframe" is advance bumps interconnect technology for Mosfet BGA.

This paper discusses the design and performance of "Copper Bump Leadframe" as it applies to MosFet BGA technology.

1.0 Introduction

The existing technology makes use of solder ball bump as the electrical interconnect in Ball Grid Array (BGA) packages. The process is widely known in the semiconductor industry as balls attach method. The solder ball bump is mechanically placed on the substrate ball land pattern using a mechanical fixture. However, various manufacturing issues take place in the integrity and quality of ball attachment. These quality issues includes the solder ball bump adhesion strength, solder ball bump coplanarity, ball size uniformity, and no ball after ball attached. The manufacturing quality issues of ball attach creates reliability failures during board application. The solder ball bump is the standard material and very popular in the semiconductor industry today. The solder alloy for the BGA interconnects is typically a near eutectic Sn-Pb alloy that melts at 183°C. The balls are fluxed and re-flowed to join to the substrate. The process is intended a no-collapse mounted solder ball. This process maintain the ball height which is very critical to ball coplanarity. Welding, or brazing, or glass sealing a lid on the die, or by flowing and curing an organic encapsulant (glob top) over the die completes the assembly of BGA package.

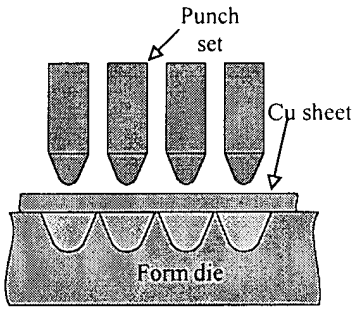


Figure 1. Punch and Die Component

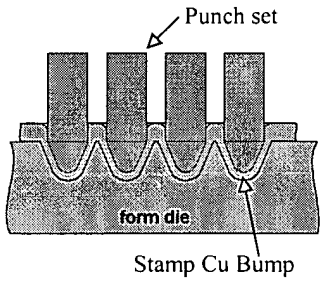
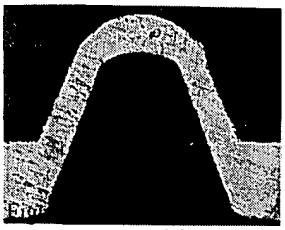


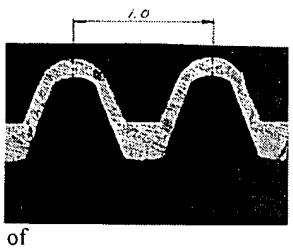
Figure 2. Full stroke stamping of Punch and Die

The "Copper Bump Leadframe" was conceptualized to advance the bump interconnect technology for Mosfet BGA and other BGA package type. The copper bump concept may also replace the traditional solder ball attach method and simplified the process of BGA packages. The

design concept 'Copper Bump Leadframe' is a result of stamping a flat, thermally and electrically conductive substrate copper material to form the leadframe with built-in copper bump. The qualification test results show an almost perfect coplanarity of the "Copper Bump Leadframe". The



sectional view of Cu bump



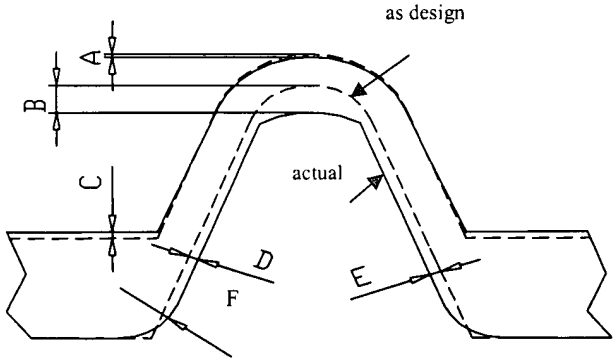
of 1.0-mm

electrical (RdSon) results for stamped copper bump is comparable to solder ball bump. It is therefore concluded that the "Copper Bump Leadframe" is an advance interconnects technology for Mosfet BGA.

The objective of this paper is to confer in detail the design and performance of "Copper Bump Leadframe" as it applies to MosFet BGA technology.

1.1 Technical Background

The copper bump interconnect is within the copper leadframe material. The copper bump is a result of stamping the flat copper metal sheet. The stamp copper bump interconnect will serve as the electrical



Legend					
a	0.027		d	0.024
b	0.192		e	0.028
c	0.019		f	0.15

Figure 5: Dimensional difference of actual bump and design

interconnection from chip to board. The spherical form of the bump is mechanically stamp by very special tools. The tools are composed of punch and die made of special steel, see *figure 1*. The punch and die is then set and assemble to punch and die assembly. The assembled die assembly is then placed into an automatic stamping press to automatically stamp the copper metal sheet. The results are then producing the copper substrate with embedded copper bump for "Copper Bump Leadframe" see *figure 2*. The most common material use in a BGA substrate is a conductive flat copper sheet metal. Any other type of material to form the bump is applicable, as design requires it to form the "Copper Bump Leadframe". A series of experimental in tooling is done to test the manufacturability of the copper bump. Since this is a new technology and never been tried before. The experiment was done in blank copper metal sheets and punches four areas for copper bump test. After the test results it is confirmed that the concept can be manufacture in volume production. The actual cross section view of initial stamp copper bump is proven the manufacturability of copper bump, see *figure 3~4*. The shape and form of copper bump is of conical in shape with spherical radius form at the tip of the bump. The conical angle of the bump is about 23° from vertical reference. The actual shape of the copper bump is then compare to theoretical design. The dimensional difference is very close and negligible, see *figure 5*. The conical design is intended for easy stamp and retraction of the tools and prevents any stuck-up after punching. The spherical form radius at the tip is the interconnection point. It is in this point that touches to the board and connected by solder paste. The electrical flow passes through the wall of copper bump through the radius tip into the board. The size and height of the bump can be configured at a desired shape depending on the requirements.

Figure 6: Leadframe Package Outline

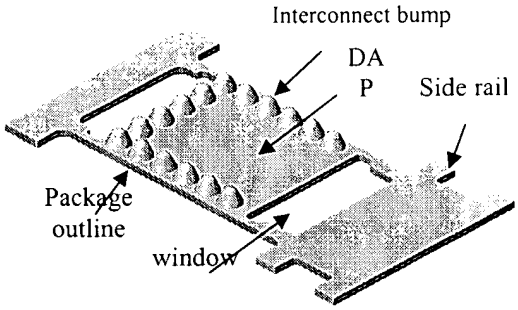
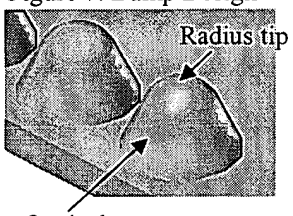


Figure 7: Bump Design



The "Copper Bump Leadframe" is a new leadframe technology that can be utilized and used for any type BGA packages. The copper bump is intentionally stamp into the copper substrate. This new concept has the potential to eliminate the traditional solder ball bump technology. The copper bump interconnect is very tough and robust in design. The coplanarity of the bump can easily be achieved since

the process is through metal stamping. The pitch of the bump can be as closed as 0.5-mm depending on the requirements. This however varies from pitch-to-pitch to different BGA packages application. Current pitch limitation is at 0.85-mm. The "Copper Bump Leadframe" as design is expected to exhibits superior electrical and thermal performance. Since the flow of electrical is trough the same copper material on any given surface-mount discrete package. The copper bump technology can be manufactured on a high-volume environment as results of initial study and experiments conducted. The design concept combines a complete process of copper substrate with stamp copper bump embedded to the same copper material. This new technology may also do away with the very complicated process of conventional ball attach method. The "Copper Bump Leadframe" is also an answer to a lead-free process, since no application of toxic lead is necessary. In order to produce the copper leadframe through stamping it will requires the following process steps. Strip feeding then downward stroke of the punch. Retraction of the punch and the copper bump is form out of flat copper metal sheet. After on cycle the blank copper sheet index to complete another cycle.

Figure 8: Backside of leadframe

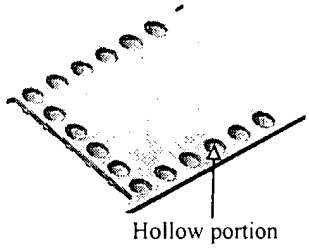
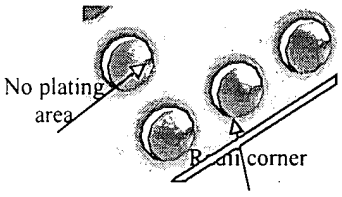


Figure 9: Bump Backside Detailed



It is then necessary to find an alternative solution for interconnects other than the conventional solder bump process. The Copper Bump Leadframe is a potential alternative solution to solder bump interconnects. The "Copper Bump Leadframe" technology has the potential to covers almost any type of BGA packages. These BGA packages include Mosfet BGA, CD BGA, Plastic BGA, and many other types of BGA packages in semiconductor industry.

2.0 Methodology

2.1 Copper Leadframe Design

The vehicle for evaluation is the 5x5.5 MosFet BGA package type. The leadframe design for copper bump is a 32-units and 5x5.5 package size and exactly pattern to MosFet BGA. The leadframe was design with stamp copper bump as feature to interconnect the chip to the board. The copper bump is an array of stamp copper bump around the periphery of the package outline, see *figure 6*. The shape and form of the "Stamp Copper Bump Interconnect" is of conical in shape with spherical radius form at the tip of the bump, *figure 7*. The conical angle of the bump is about 23° from vertical reference. The conical design is intended for easy stamp and retraction of the tools and prevents any stuck-up after punching. The spherical form radius at the tip is the interconnection point. It is in this point that touches to the board where the electrical flow passes through into the board. The size and height of the bump was configured at a desired shape as per specification of the bump design requirements. The backside of the leadframe is an array of hollow portion. This hollow portion at the backside of the bumps is the results of stamping blank the copper metal sheet, see *figure 8*. However, the hollow portions posses a big problem on plating. An expose copper is very visible after plating in lowest tip area of the hollow, see *figure 9* for detailed view. The plating process failed to cover the area. The reason for this is the absence of chemical reaction in this portion. Final design shape of the bump is shown in *figure 10*.

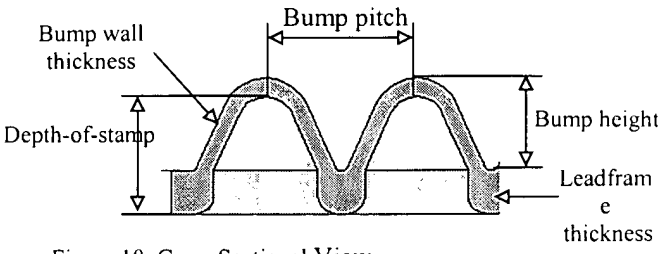


Figure 10: Cross Sectional View

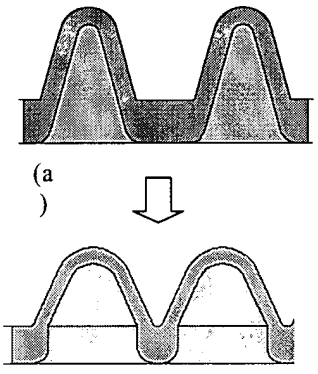


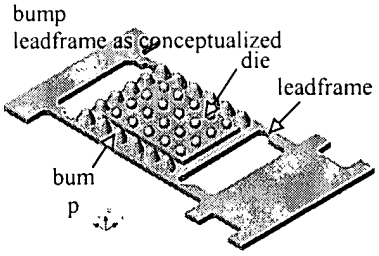
Figure 11a~b: Shows design option for Cu bump

2.2 Detailed Copper Bump Design

In *figure 10*, shows an optimized shape of the copper bump as it passes several design concepts. The pitch of the bump is 0.85-mm on the Y-axis while the pitch on the X-axis is about 0.80-mm. The height of the bump is as required is 0.533-mm. The optimized height is compensated to the height of the flip chip plus the bond line thickness of 0.0254-mm. The plating is full nickel-palladium plated. *In figure 11a*, shows the initial design concept of the bump. The conical shape is too small and

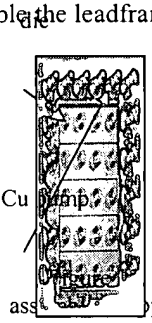
slender. It will require a very small tooling in order to produce the parts. If the design will be push-through the cost of tooling is very high and the quality of the stamp bump will be very poor. The stamping punch in this design concept becomes very long and thinner. During the fabrication the punch is prone to breakage. Upon thorough review and study the initial design was then dropped in favor of improved design concept as shown in *figure 11b*. The bump is bigger in size comparing to previous design. The punch may last into production of leadframe and may results into a better quality of stamp copper bump. The final design is then considered for tool-up then applied to run for prototype. The final design should also considered to be manufacturable, either be in leadframe manufacturing or in assembly process.

Figure 12: Assembled copper bump leadframe as conceptualized



2.3 Assembly Process

The copper bump leadframe is then assembled. The device used to assemble the leadframe is 5VCEA type of device. Total number of units per leadframe is 32-units, then assembled 24-strips. The assembled units will determine the total height of the package thickness including the ball height. This will also determine the coplanarity of solder bump and copper bump in same level of plane. The assembly process will follow exactly as per design concept, see *figure 12*. A soft solder process is applied during die attach, with a bond line thickness of 1-mil. In *figure 13*, shows the actual assembled unit. The die-attached solder is wetting very well as it reaches the copper bump edge. The copper bump leadframe is thinner by 8-mils. During die attach process it encounter jamming. The frame tends to bend during indexing. This cause by insufficient height of tensioner pins. This encountered problem was quickly resolved by adjusting the tensioner height to satisfy the new thickness of leadframe. Original setting of tensioner is at 12-mils leadframe thickness. The wetting of soft solder reaching the Cu bump is maybe because of the absence of groove at the die pad area. The issue can be resolved by adding a groove or dimple at leadframe pad.



Actual photo of ass pper bump leadframe

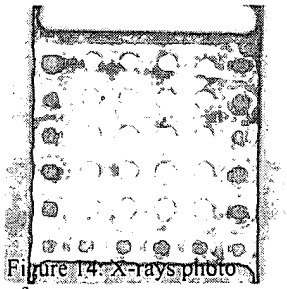


Figure 14: X-rays photo of Die attach pad

2.4 Voids Inspection after Die Attached

The assembled unit is then inspected of voids after die attach process. This to determine the presence of trapped air on the pad area. This area is one factor to determine the bondability of die and to maintain the bond line thickness of solder paste within 1-mil. In *figure 14*, shows the picture of the package after the x-rays. The picture shows no evidence of voids in the die, and the parameter used for die attach are the same as the standard MosFet BGA.

2.5 Electrical Test

Two lots will be tested for electrical performance under the following electrical parameter condition, see *table 1*.

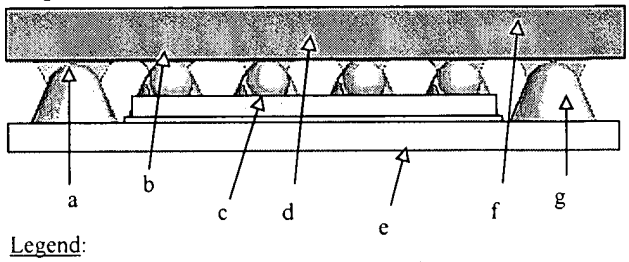
Table 1. Electrical test control limit

Control Lot 1	122	
Control Lot 2	173	
Condition 1	4.5V	10V
Condition 2	18A	22A
Max Limit	0.0047	0.0033
Min limit	none	none
Unit	mR	mR

2.6 Board Mounted Units

The assembled units are then mounted to the demoboard to test for coplanarity and other reliability. In *figure 15*, shows the ideal board mounted units. The copper bump and solder bumps are perfectly lying on the same plane and all bumps are covered by solder paste

Figure 15: Ideal board mounted unit



Legend:

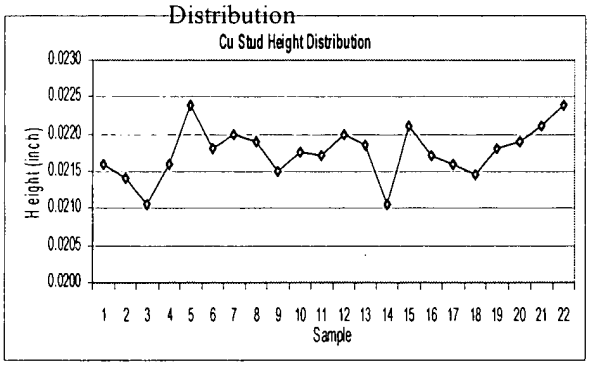
a. Copper bump
b. Die
c. solder bump
d. bond line
e. chip board
f. copper leadframe
g. solder paste

3.0 Results and Discussion

3.1 Coplanarity Measurements for Bumps

The bump height of the leadframe bumps was then measured to determine the coplanarity of the bumps. The bump height coplanarity is very critical in MosFet BGA. Non-coplanar bumps may results into non-contact portion to the board. This may effect the overall electrical results of the unit. *Table 2*, shows

Table 2: Copper Bump Height Distribution

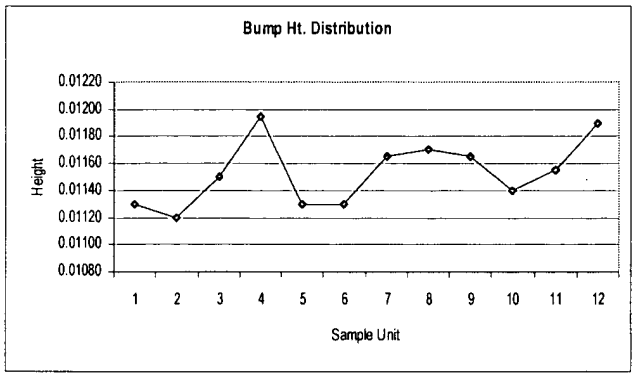


the Cu stud height variation from unit to unit. The height varies from 21.05-22.40 mils to a target of 21.0 mils. The Cu stud height is based from die thickness of 8-mils. Then add the bump-nominal height of 12-mils. Then add the bondline thickness of 1-mil. The computed height gives a total of 21-mils overall height. The height variation of copper bump is at 1.35-mils.

3.2 Wafer Solder Bump Height Characterization

The solder bump is also been measured and characterized to determine the bumps coplanarity. This measurement is very important in the

Table 3: Wafer Solder Bump Height Distribution

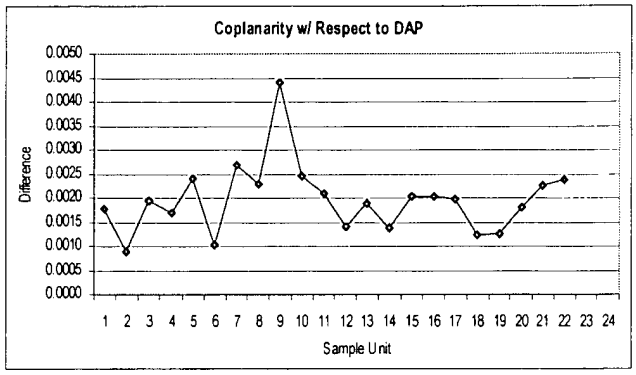


computation of required bump height design to leadframe. In *table 3*, shows the bump height variation from die-to-die. The solder bump height is measured at 11.2 to 11.95-mils. The solder bump height specs is at 12-mils. From the data, there is no significant height difference between gate and source.

3.3 Coplanarity Measurements of the Package

In *Table 4*, show the results of coplanarity measurements with respect to solder bump and copper bump height measurements. The die attach pad as reference. The total

Table 4: Coplanarity Measurements

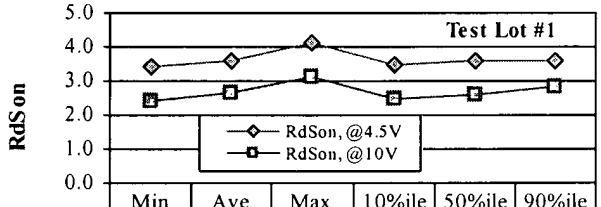


height of the die plus solder bump, plus bondline thickness of 1-mils is 20.19-mils. The height of the copper bump by design is at 21-mils. The average coplanarity of the solder bump and the copper bump range at 1~2-mils. This shows the almost perfect planarity of copper bump, with respect to solder bump height

3.4 Electrical Test

The electrical test was conducted to determine the functionality of the bump. Since the copper bump is a hollow with very thin wall. There is some doubt whether

Table 5: Electrical Test Result, Lot #1

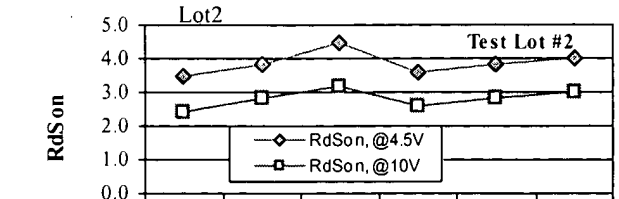


	Min	Ave	Max	10%ile	50%ile	90%ile
RdSon, @4.5V	3.4	3.6	4.1	3.5	3.6	3.6
RdSon, @10V	2.4	2.7	3.1	2.5	2.6	2.8

the unit will perform the same as the standard MosFet BGA. The results of the electrical test will determine the affectivity of the copper bumps comparing to standard solder bump. The results of electrical parametric test show a comparable performance to standard MosFet BGA, *table 5~6*. The actual RdSon electrical reading of copper bump is at 3.5~4.0 mR @4.5V, and 2.4~3.2-mR @10V. Ninety percentile of the reading is at 4-mR and 3-mR respectively. The current carrying capacity of the copper bump was not measured due to unavailability of

measuring equipment. Several attempts were made to measure the carrying capacity of the copper bump, but failed to provide positive results.

Table 6: Electrical Test Result,



	Min	Ave	Max	10%ile	50%ile	90%ile
RdSon, @4.5V	3.5	3.8	4.5	3.6	3.8	4.0
RdSon, @10V	2.4	2.8	3.2	2.6	2.8	3.0

3.5 Board Mount Testing

In *figure 16~17*, shows the actual unit mounted on the board. It is apparent that copper bump and the solder bump are lying on the same plane of the board. The actual chipboard is 1-in^2 type of demo-board. The unit was then manually mounted to the board. The solder paste used is a 6337 type of solder paste or 63% Tin and 37% Lead. The assembled unit was then process in I/R re-flow oven. After the re-flow the mounted unit is inspected for adhesive strength and check for accurate position.

Figure 16: Actual board mounted unit

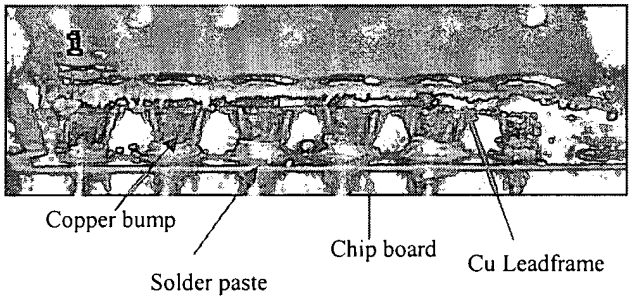
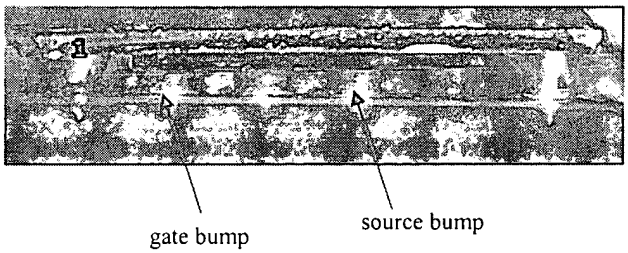


Figure 17: Gate bump and source bump connection



4.0 Conclusion

1. The results of the parametric electrical test show comparable performance of copper bump comparing to standard solder bump ball attach concept. The actual RdSon electrical reading of copper bump is at 3.5~4.0 mR @ 4.5V, and 2.4~3.2-mR @10V. Ninety percentile of the reading is at 4-mR and 3-mR respectively.
2. The current carrying capacity of the copper bump was not measured due to unavailability of measuring equipment.
3. The thermal test result shows a 5% higher comparing to standard. However, the 5% thermal difference is not that significant to affect the performance specifically the wireless application
4. The board-mounted unit shows the copper bump, source solder bump, and gates bump are all in the same level plane.
5. This design concept will also simplified the process of BGA technology by eliminating the ball attach process
6. It is therefore concluded that the "Application of Copper Bump Leadframe" will advance the manufacturing and technical reliability MosFet BGA Technology.

5.0 Recommendation

1. Continue to develop the simulation software to determine the current carrying capacity of the copper bump
2. Search for new leadframe material to improve the thermal performance of the copper bump
3. Optimized and improved the plating process to fully cover by plating the backside of hollow portion of the bumps
4. Continue to develop into a finer pitch of 0.65-mm and bump height of 0.25-mm, using a 0.25~0.30-mm thickness leadframe
5. Add V-groove at pad area to control the flow of soft solder during die attach
6. Continue to rebuild more samples for reliability testing

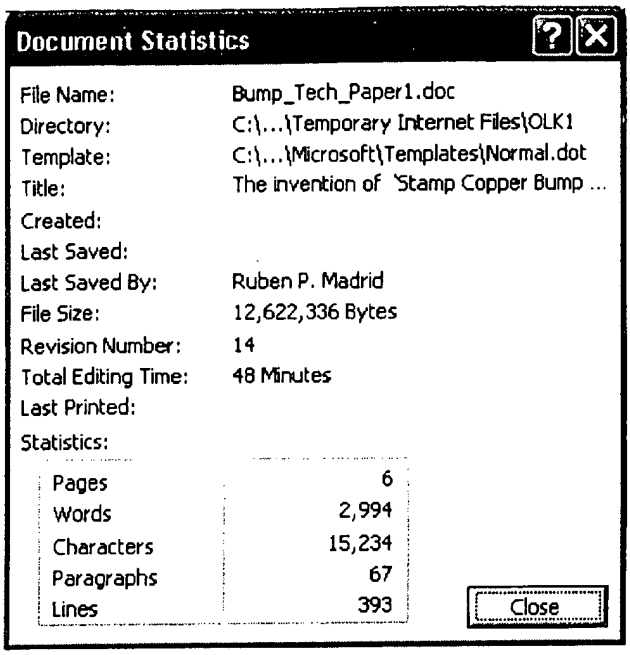
6.0 Acknowledgment

The authors would like to express thanks and deep gratitude to the following people.

1. Connie Tangpuz – Product Technology Group Manager for her strong push to complete the technical paper
2. Rajeev Joshi – Director of Packaging Technology Group, Worldwide for his consideration in the importance of this paper
3. Arniel Jaud – for the drawing requirement for MosFet BGA

7.0 References

1. Internet Web Site for Solder Bump Technology
2. In-house drawings by Product Technology Group, Fairchild Semiconductor
3. GOTOH reference drawings,.


Document Statistics
File Name: Bump_Tech_Paper1.doc
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Lines 393
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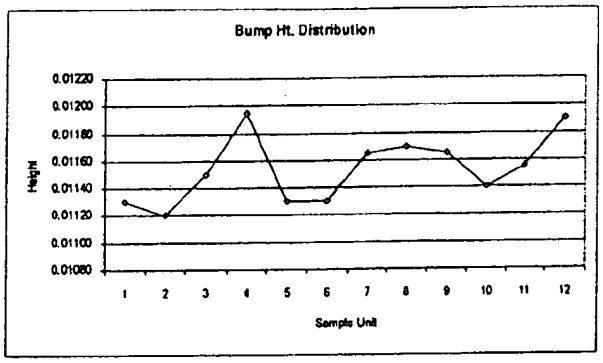
MOSFET BGA Cu STUD EVALUATION

Purpose: To evaluate, characterize and qualify Cu bumps on MOSFET BGA package as an alternative to high lead solder sphere.

Background: The existing design of MOSFET BGA uses high lead solder spheres as drain interconnect to the PCB. These solder spheres are attached to the array of dimples in the leadframe. The dimple depth & diameter variation is very difficult to control due to etching process & leadframe thickness. These two dimensions are very critical for this package. To resolve such variation, the Cu stud concept came into idea.

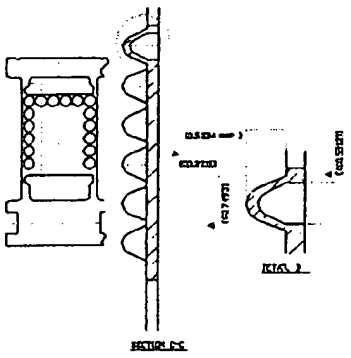
Results and Discussion:

1. **Wafer Level Characterization**
   1.1. Bump height

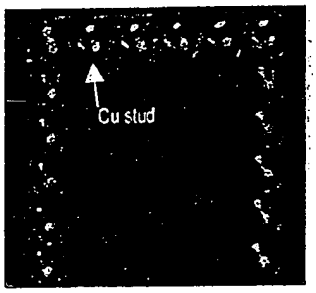


Remarks: The graph above shows the bump height variation from die to die. The height is running at 11.2-11.95 mils from a target of 12.0 mils. There is no significant difference noted on the bump height difference between gate & source.

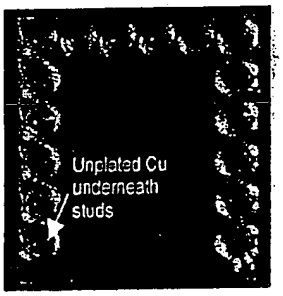
2. **Leadframe**
   2.1. Visual



Design



Top portion

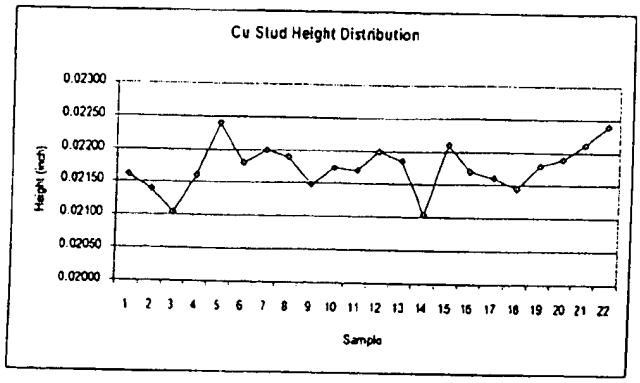


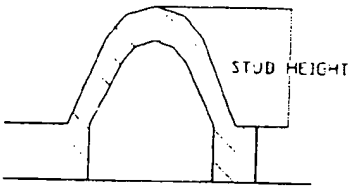
Back portion

Actual

Remarks: The actual parts have exposed Cu underneath the studs due to entrapped air during plating process. The correct process has not been defined yet to plate through the stud opening of 0.551mm and a depth of 0.533mm. The frame thickness is 10 mils. The strip is plated with Full Ni/Pd.

2.2. Cu Stud Dimensional





Remarks: The graph above shows the Cu stud height variation from unit to unit. The height varies from 21.05-22.40 mils from a target of 21.0 mils. The Cu stud height is based from die thickness + bump nominal height + bondline thickness which in this case is 8mils + 12 mils + 1 mil respectively.

After Soft Solder Die Attach

3.1. Solder Composition: Sn8.5Sb

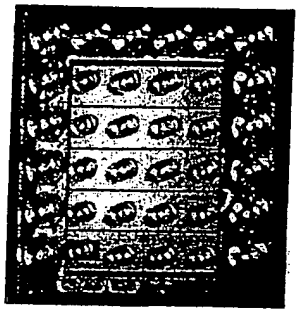
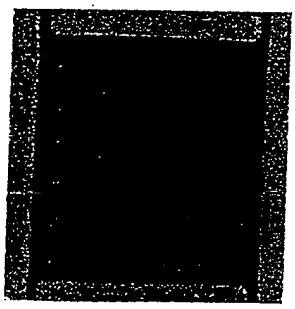


Photo shows a die attached Cu stud. The die attach solder seem to wet well, reaching the Cu studs.

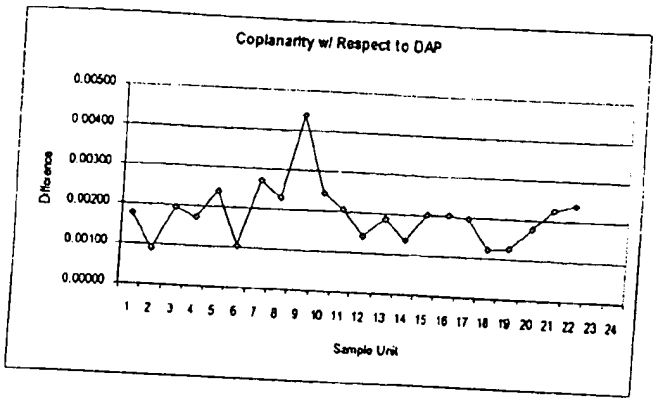
Remarks: Jamming problem was encountered during die attach process. The frames tend to bend during indexing. This is caused by insufficient height of the tensioner pins to index the frames since the frame thickness is reduced to 10 mils from the current of 20 mils. To resolve such, we need to adjust the pin height & sharpen the pin tips.
The solder reaching the Cu studs, though is not issue electrically, maybe resolved by adding a v-groove to contain the solder.

.2. Die attach voids inspection



Remarks: There were no die attach voids seen on the x-ray results using the same settings as the standard packages.

4. **Coplanarity Measurement**



Remarks: A stud-to-bump coplanarity of 1-2 mils is expected from a stud average height of 21.76 mils and a total die height (die thickness + bump height + bondline) of 20.19 mils.

Electrical Testing

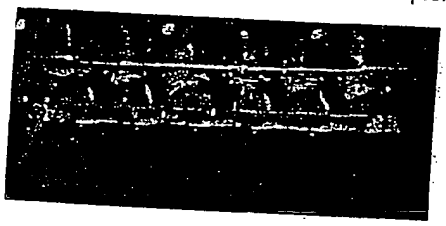
5.1. The parametric test results on the Cu studs shows a 0.1-0.2 mohm difference in Rds(on) compared to the drain ball interconnect. The readings measured are 3.5-4.5mohm @ 4.5V and 2.4-3.2mohm @ 10V. Ninety percentile of the readings are at 4mohms and 3mohms respectively.

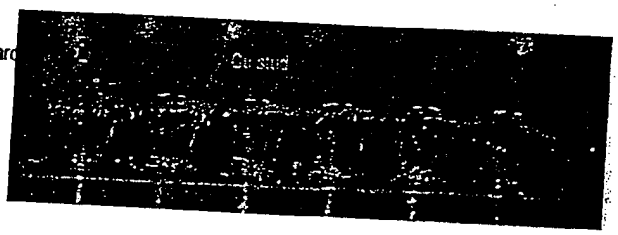
5.2. The difference in the current carrying capability was not measured because there is no capability in-house. A few samples were forwarded to the product engineering group in the US to determine the thermal as well as check for any current degradation if there is any.

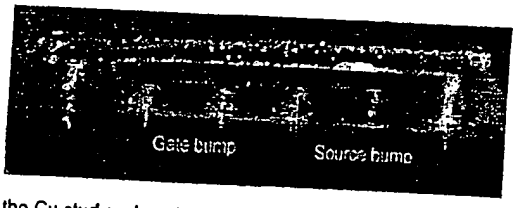
Board Mounting

6.1. Solderability test

Remarks: The photos above show the Cu studs after manual board
The studs are wetting quite well to the eutectic paste.







Remarks: The photo shows the Cu stud coplanarity with the solder bumps after board mount. All bumps (gate & source) are in contact with the solder paste.

7. **Action Plans**

Action Item	Remarks
1. Package Simulation	▪ Perform a package simulation in Fairchild Korea software while waiting for Gintic simulation.
	▪ Good units (100 pcs) will be forwarded to Gintic for the package simulation study. These parts are awaiting availability of mounting boards designed by Gintic.
2. Thermal & current capability measurement	▪ Good units (50 pcs) forwarded to product engineering group in the US
3. Exposed Cu	▪ Optimize pre-treatment process during plating in the next batch of materials
4. Leadframe jamming	▪ Convert to 0.3mm frame thickness since Gotoh confirmed they can still meet the 0.85mm pitch & 0.533mm height.
	▪ Redesign tensioner to cater to 0.3mm frame thickness.
5. Stud pitch & height for smaller packages	▪ Gotoh confirmed that they could meet the 0.25mm stud height & 0.65mm pitch using a 0.25-0.3mm frame thickness.
6. Die attach solder reaching Cu studs	▪ Plan to add v-grooves to contain the solder.
7. Board level reliability test	▪ Rebuild samples for rel testing.